REMARKS

[1] The Examiner required that Figs. 1-2 be labeled as prior art. This has been done.

The Examiner also objected to the drawings for not showing the feature of larger non-doped area. This feature is shown in the amended Figs. 3(a)-3(c) and the specification is amended to explain how the drawing change now better illustrates the feature.

The rejection is respectfully traversed for the record, on the basis that one area being larger than another area is a simple concept, understandable without specific illustration.[1]

[2] Claim 1 was objected to. Correction is made as required.

[3] The claims were rejected under §112, second paragraph. The claims are amended in view of the Examiner's remarks and withdrawal of the rejection is requested.

[4] Claims 1-4 were rejected under §103(a) over Brown '269 in view of Morihara '506. This rejection is respectfully traversed.

When a polysilicon layer is simultaneously etched in order to form dual gate electrodes, it is conventional that all of the polysilicon layer is doped to be either N-type or P-type. The Applicant claims additional non-doped regions, where the non-doped regions occupy an area larger than the doped regions. When the polysilicon layer is etched, this results is improved gate shapes, because the polysilicon etching strongly depends on the area of non-doped polysilicon regions.

The Examiner is invited to consider:

---

[1] 35 USC §113 requires illustration "where necessary for the understanding of the subject matter."

(1) The Examiner admits (page 4, last paragraph) that Brown does not disclose a larger non-doped area. However, the Applicant notes it is not only a *larger* area that is not disclosed by Brown: no non-doped region whatsoever is disclosed.

(2) The Examiner relies on Morihara for the missing features. Morihara is concerned with uneven feature development due to electric charge buildup, a condition that occurs near to edges of circuit areas (¶[0014]), and Morihara solves this problem with a wafer in which the partial squares at the edges are printed with dummy circuit patterns in order to maintain a constant wiring pattern density over the surface of the wafer. The dummy pattern area is called a "component agenesis field 3" and the chip areas are called "component formation field 2" (¶[0021]). Morihara explains that the density is constant over areas 2 and 3 (¶ [0022], abstract). No disclosure of polysilicon (whether doped or un-doped), nor any mention of areas,[2] is seen.

(3) The Examiner asserts that Morihara's feature 21a is a dummy gate made of non-doped polysilicon (Action at page 4, last line). However, ¶[0028] mentions "dummy pattern 21 which consists of electric conduction film 8b and silicon oxide 7b," and this description is not consistent with the claimed un-doped polysilicon.

With respect, Morihara does not actually disclose any un-doped polysilicon regions, nor any doped polysilicon regions, nor any area ratios between such regions. Morihara is concerned with circuitry and does not even mention doping anywhere in the reference.

(4) Because Morihara does not disclose the features of the claims, no combination of the references, even they were obvious to combine (not admitted), could possibly lead to the Applicant's claims.

---

2 A density if a ratio of areas, so area *per se* is independent of density.

(5) The teaching of applied paragraph [0022] is that the dummy region 3 are similar to the non-dummy regions 2, in that the ratio of wiring area to non-wiring area is the same in both. In general, the gist of this reference is that the dummy areas are *not* different.

Thus, the non-wiring areas in the dummy region 3 are in proportion to the corresponding areas in the non-dummy region 2. Even if the teaching of Morihara on wiring areas were applicable as a teaching on areas of doped and un-doped polysilicon (this is not admitted), the teaching would still be to make everything *the same* everywhere, and not to make un-doped areas larger.

(6) The dummy patterns are not contiguous with the circuit patterns, being separated from them by score lines. Also, the dummy non-wiring areas are not contiguous with the non-dummy wiring areas. The amended claims recite areas that are contiguous, and this feature is not disclosed, no matter how the reference is interpreted.

(7) The Applicant points out that Brown deals with the same problem as the Applicant, namely, differences in the N and P type gates (instant specification, page 4 above Summary section; Brown at col. 2, line 19). However, Brown presents a completely different solution to the same problem, and therefore teaches against modifying Brown to again solve the same problem.

(8) The Examiner asserts that the person of ordinary skill would have combined Morihara with Brown "to reduce dispersion ... of a circuit pattern." However, Brown is not concerned with circuit (wiring) patterns nor with their dispersion. Brown deals only with N type and P type transistor gates (col. 1, lines 7-11; col. 2, lines 53-55).

[4] Claim 5 was rejected under §103(a) over Brown '269 in view of Morihara '506 and further in view of Lee. This rejection is respectfully traversed.

The Examiner points out (page 2, line 10) that Lee teaches using a gas mixture to obtain identical etching behavior. With respect, this teaching is a teaching against combining Lee with Brown, because Brown teaches a different approach to the same problem (and neither suggests the Applicant's approach). If two references each taught a different solution to the same problem, the person of ordinary skill would have had no reason to combine them, because either one alone had already solved the problem.

Withdrawal of the rejections and allowance are requested.

Respectfully submitted,

July 12, 2005
Date

Nick Bromer (Reg. No. 33,478)
(717) 426-1664
RABIN & BERDO, P.C.
CUSTOMER NO. 23995
Telephone: (202) 371-8976
Telefax : (202) 408-0924